Research Article *Energy, Environment and Storage* (2022) 02-02:31-40

Energy, Environment and Storage

JournalHomepage: www.enenstrg.com

Bulk Switched DC-DC Buck Converter

Seyfettin Gürel[1], Sezai Alper Tekin[2*]

[1]*Energy Market Regulatory Authority (EPDK),Ankara, Turkey* [1]*ORCID:0000-0001-8504-2784*

[*2]*Department of Industrial Design Engineering, Erciyes University, Kayseri, Turkey*[*2]*ORCID:0000-0001-5860-2758*

ABSTRACT. This paper presents a buck converter which has an high efficient and low power consumption for low power applications. The proposed topology is based on buck converter using switching MOSFET with bulk-terminal. The suitable bulk-terminal switching voltage is selected by analyzing the effect of bulk voltage on a MOSFET performance. It is concluded that the bulk-switched DC-DC buck converter structure has the advantages such as high switching performance, low power consumption and high efficiency compared to conventional DC-DC converter circuits. The efficiency value has obtained 88.2%. The proposed circuit is approved experimentally and simultaneously.

Keywords:CMOS Integrated Circuits, Converters, DC-DC power converters, .Solar Power Conversion, Switching Converters

Article History: Received: 22.02.2022; Revised: 11.03.2022; Accepted: 26.04.2022; Available online: 26.04.2022

Doi: https://doi.org/ 10.52924/BCMQ4493

1. INTRODUCTION

In recent years, renewable energy systems have been popular whereas the fossil fuel based conventional system has the negative effect on the environment and human health. In addition, it is also important to transport and store the energy in these systems in the most efficient way. Therefore, scholars have been focused on the design systems used as being more efficient and sustainable. The converter circuits are a very critical importance in terms of efficiency because the voltage and current parameters need to be converted for storing and transporting. The converter circuits can be defined as structures that efficiently convert voltage and current levels of generated electrical energy to significant levels to be used in power systems [1]. Additionally, DC/DC converters using for low power applications constitute the backbone of diverse portable electronic devices such as smartphones, laptops, navigation devices and automotive electronics which are using batteries as their power supply. Portable devices ordinarily consist of several sub-circuits that should be supplied with different voltage levels which is the main supply voltage [2]. There are many workings in the literature about DC-DC Converter applications such that it can be used in various areas such as communication systems, energy har vesting circuits for solar systems and piezoelectricapplications. Piezoelectric harvesting circuits are attractive because it can be said that these circuits make easier energy harvesting from piezoelectric material by matching load impedance with source impedance in circuit. This is also called maximum power point in which the circuit operates with maximum output voltage. Then, the maximum power transfer can be available from harvesting circuit. Optimizing with these parameters, the buck harvester circuit has high output voltage and high switching speed that can be designed for piezoelectric devices [3,4]. Hence, there are many kinds of converters which are suggested for different voltage ranges by researchers [4-9]. An off-grid with lead acid-based battery PV system is designed for the system. The charge status of battery is arranged with MPPT technique. It is specified that there is an improvement in PV performance which is simulated with DSP card design. There may be shading and mismatch conditions due to the interconnection of PV panels. To solve this problem, distributed MPPT system with synchronous buck converter is proposed for increasing efficiency [10, 11]. As indicated in the above, many designs of innovative converters are mainly related to reducing the dimensions of circuit components, area and the total weight of circuit design for mobile systems.

These parameters can be resized when it is available new devices that operate at high switching frequencies. The suggested buck converter design is composed of main circuit and the control unit for control-ling the microprocessor via opto-coupler [12].

The converter topology which exists in literature also takes place in data communication systems. It is possible to reach high power levels and data rates for these systems

*Corresponding author: satekin@erciyes.edu.tr

[13]. The minimization of losses is the most important topic for designing converter circuits. In the literature, there are many designs and techniques offered by a scholar to diminish the switching stress and losses in different converter designs [14-17]. On the other hand, there are many studies about algorithm-based DC-DC Converter designs, but it is not enough studies that focusing switching loses circuit design for buck converters. there are few workings about the circuit and transistor structures in the literature [16].

The present study is aimed to bulk controlled DC-DC buck converter that reduces transistor switching losses using bulk terminal of a MOSFET. The main aim of this study is to design a DC-DC buck converter which has less power consumption than the current state-of-the-art studies available in the literature. Circuit designs which consist of transistors with four terminals are available in literature related with low-power applications and microelectronic circuit designs [26, 27]. However, it is not encountered converter applications in literature. Besides, there are not many studies about the suggested converter which includes low power circuit structures. The clear contribution of this design is to have low power consumption and operate at low-er duty cycle compared with other converter topologies in the literature. In this study, it is intended to design the DC-DC buck converter which is simple and effective without changing the fundamental structure of buck converter. The classic and proposed buck converter designs are examined and performed as a simulation and experimentally. Additionally, the proposed and other converters which are given in literature are compared with respect to performance criteria. Eventually, the proposed design can contribute positively to the converter structures.

2. THE CONVENTIONAL BUCK CONVERTER

A classic buck converter is shown in Fig. 1. During the design process of converter structures, the structure of the topology is very important to validate and analyze the operation of the circuit.

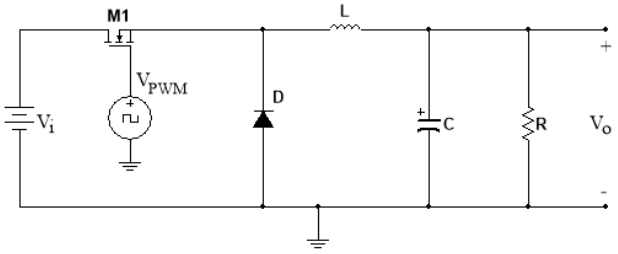

Fig 1. The conventional DC-DC Buck Converter.

The mathematical equations for this converter can be given as Equation (1-3):

$$V_i(t) = V_o(t) + L \cdot \frac{di(t)}{dt}$$

$$i_L(t) = \frac{1}{L} \int (V_i(t) - V_0(t \quad (2)$$

When it is applied KVL and KCL in the Fig. 1, it is obtained as follows:

$$i_c(t) = i_L(t) - i_R(t) \quad (3)$$

2. PROPOSED CIRCUIT DESIGN

2.1 The Switching of MOSFET

There is a duration that is necessary for operating MOSFET in the cut-off region or out of this region. In converter design, the core of the converter is the MOSFET which is the semiconductor device to control the whole system. The on-period duration changes the values between maximum and minimum values of the duty cycle (D). The output voltage varies with this duty cycle. Also, the switching frequency is reversely proportional with voltage ripple in load. For reducing ripples, the frequency should be increased [19]. The frequency of MOSFET is most important parameter for designing desired input and output voltages. When the frequency boosts up, the power consumption also ascends. Besides, the amount of power consumption reaches its highest values in falling and rising times of MOSFET. For this reason, it becomes very important to deal with this effect via using different strategies.

The bulk terminal of MOSFET is usually connected to source terminal. In this manner, it is tried to eliminate the body effect parameter. However, the body effect can be considered as an advantageous for the MOSFET. Therefore, it is also possible to use bulk terminal of MOSFET. The MOSFET's threshold voltage V_{TH} is given by Equation (4) [20].

$$V_{TH} = V_{T0} + \gamma \cdot [\sqrt{|2\varphi_F| - v_{BS}} - \sqrt{|2\varphi_F|}] \quad (4)$$

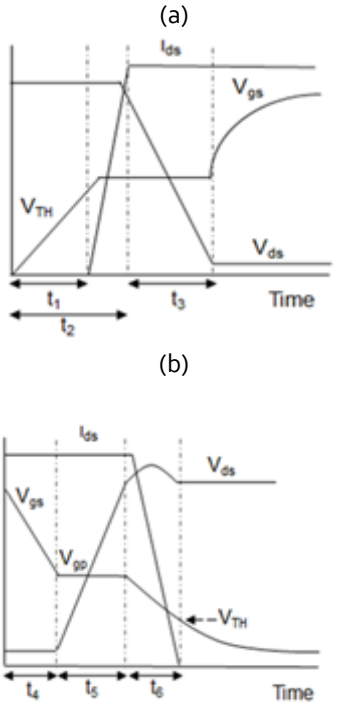

Fig. 2(a). A turn on transient of the MOSFET; **(b)**. A turn off transient of the MOSFET

In Equation (4), γ is the factor of body effect, V_{BS} is the voltage of bulk-to-source voltage, V_{T0} is the threshold voltage when V_{BS} =0, φ_F represents the change in the surface potential, respectively [21]. From the equation

(4), it can be said that increasing with V_{BS}, the value of V_{TH} decreases. Hence, a drain current ID increases and a drain resistance R_D decrease during operation of the MOSFET.

The MOSFET has been used as a switching device. To make switching process, it has been used PWM signal. PWM signal is preferable since it has been given an ability to control on the system. The turn-on and turn-off characteristics which are called switching time for the MOSFET is displayed in Fig. 2(a) and (b) [22].
The length of the switching time has a negative effect on the power consumed by the transistor. The shorter switching time can reduce the power consumed by the transistor. That is why, this power dissipation should be lessened. In rising time, the switching time faster and more efficient than in falling time because the effect on applying V_{BS} voltage has a positive impact on MOSFET performance in rising time. However, the same situation is not possible in falling time for MOSFET because the power dissipation occurs due to the absence of good switching characteristics in this duration. Therefore, the adaptive circuit design is needed for reducing the undesirable effect of this structure.

$$t_1 = R_G \cdot C_{iss} \cdot ln\left(\frac{1}{1-\frac{V_{TH}}{V_{GS}}}\right) \quad (5)$$

where C_{iss} is input capacitance, V_{GS} is gate-to-source voltage. Also, R_G is the resistance of drain terminal. t_1 isthe time where V_{TH} is only the parameter for switching the MOSFET in Fig. 2a.

$$t_2 = R_G \cdot C_{iss} \cdot ln\left(\frac{1}{1-\frac{V_{GP}}{V_{GS}}}\right) \quad (6)$$

where V_{GP} is gate to plateu voltage. Ciss is input capacitance. t2 is the duration where V_{GP} and V_{GS} are two parameters which determine the length of this duration.

$$t_3 = R_G \cdot C_{gd} \cdot \left(\frac{V_{DS}}{V_{GS}-V_{GP}}\right) \quad (7)$$

in which V_{DS} is the drain-to-source voltage. t_3 is the time where V_{DS} , V_{gp} and V_{GS} constitute this duration. C_{gd} represents gate-to-drain capacitance.

$$t_4 = R_G \cdot C_{gd} \cdot ln\left(\frac{V_{GS}}{V_{GP}}\right) \quad (8)$$

t_4 is the duration where only the effect of V_{GS} parameter is dominant. C_{gd} represents gate-to-drain capacitance.

$$t_5 = R_G \cdot C_{gd} \cdot \frac{V_{DS}}{V_{GP}} \quad (9)$$

t_5 is the time where V_{GP} and V_{DS} are effective. C_{gd} represents gate-to-drain capacitance.

$$t_6 = R_G \cdot C_{iss} \cdot ln\left(\frac{V_{GP}}{V_{TH}}\right) \quad (10)$$

t_6 is the duration where V_{TH} affects the duration of this time. V_{TH} is threshold voltage of the transistor. C_{iss} represents total input capacitance.

From Equation (4), it can be observed that when the bulk-terminal voltage increases, the rising time shortens. By considering this approach, it can be commented that V_{BS} is lessened in the rising time. When the bulk-terminal voltage is increased, the power consumption is also decreased in rising time. However, the bulk-terminal voltage expands falling time, the power consumption is also increased in failing time because the high V_{BS} voltage values adversely impact the switching time of the MOSFET in falling time and it causes the increase in power consumption in MOSFET. In rising time, the bulk-terminal voltage should be increased. Whereas, V_{BS} must be decreased in falling time.

2.2 Buck Converter Circuit Design

The buck converter is shown in Figure 3. It is the common topology for employing power distribution cir-cuits, development boards, etc. It ensures the required local voltage values from higher voltage values in the system. A typical converter includes an active and controlled switch, rectifier elements (diode e.g.), ca-pacitors and inductors. The basic structure of the con-verter permits the achievement of high efficient power characteristics with the design. The buck converter contains the inductor on the output of the buck con-verter that yields a regulated output current to the load. This seems to beadvantageous in terms of achieving high efficient converter design. However, some specific conditions may appear, and these issues should be taken into consideration during the design procedure. The input is applied to switching device and the behavior of input current has active waveform. This situation has the negative effect on converter since the controlled current spreads out the noise into all system. To eliminate this undesired impact, the appropriate decoupling is indispensable for converter. Therefore, capacitor is an important portion of converter structure.

It was also promising for applying this idea to the buck converter topology. When the basic structure of buck converter is simple, the extra advantage of the effect of bulk terminal voltage for buck converter has become more competitive comparing with converter structures.

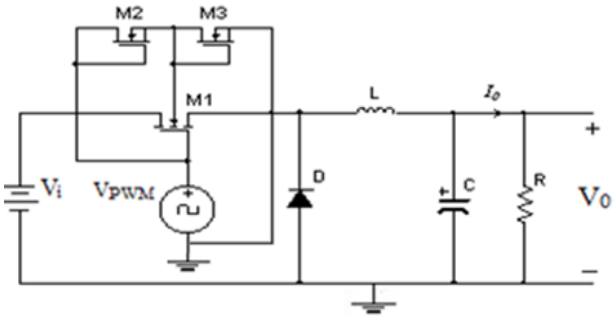

Figure 3. The proposed DC-DC Buck Converter

Two circuit topologies are analyzed and examined for understanding the effect of bulk-terminal voltage on a proposed DC-DC Buck Converter. Each circuit is analyzed and simulated with PSPICE. The proposed converter has depicted on Fig. 3. Transistor M_1 that has

four terminals is switching element. M_2 and M_3 connected bulk terminal of M1 are voltage divider circuit. There are M_2 and M_3 MOSFETs that represent resistors in the voltage divider circuit.

A low amplitude voltage that is synchronized with the PWM signal VPWM is applied to the bulk terminal of M1 by the voltage divider circuit. Thus, the threshold voltage of the transistor M1 is changed simultaneously with the PWM signal. The W/L equations wereformulated for TSMC 0.13 μm technology. Drain currents I_{D2} and I_{D3} for M2 and M3 given as,

$$I_{D2}=\frac{1}{2}k_n\frac{W_2}{L_2}\cdot(V_{GS2}-V_{TH2})^2 \quad (11)$$

$$I_{D3}=\frac{1}{2}k_n\frac{W_3}{L_3}\cdot(V_{GS3}-V_{TH3})^2 \quad (12)$$

where I_{D2} and I_{D3} are drain currents of M2 and M3 respectively. V_{GS2} and V_{GS3} are gate-source voltages, W_2/L_2 and W_3/L_3 are aspect ratios of M_2 and M_3. The transconductance parameter represents kn. Also, V_{TH2}, V_{TH3} are the threshold voltages of M_2 and M_3, respectively. Because M_2 and M_3 are identical, then, $V_{TH2}= V_{TH3}$ and $I_{D2}=I_{D3}$. Also, $V_{GS2}= V_{PWM} - V_{BS}$ and $V_{GS3}= V_{BS}$ where V_{BS} is equal to V_B-V_S as shown in Figure 3. V_{PWM} is PWM voltage. Therefore, the equation can be written as bulk-source voltage V_{BS} of M_1:

$$V_{BS}=\sqrt{\frac{2I_{D3}}{k_n(W_3/L_3)}}+V_{TH3} \quad (13)$$

wherein the bulk current has been neglected because it is very small compared to I_{D2}.It is also important to determine ideal value of inductor L and capacitor C for the proposed converter because the voltage or current which is charging on capacitor or inductor may reduce the output voltage or output current. The next step is to calculate the duration in which the switch is ON, OFF and total time in DC-DC Buck Converter Design. In the proposed design, input voltage is selected as V_i=10V and the output voltage is selected as V_0=3.3V. The output voltage is adjusted as 3.3 V because many electronic systems such as microprocessors, communication and mobile application systems work with 3.3V. Therefore, it is preferred this voltage level. Also, the input voltage can be selected at a different value. For these requirements, the inductor value, switching frequency, the capacitor value is calculated via formulas. The value of inductor and capacitor calculations are given as in detail as Equation 14 and 15.

The inductor value which is used in circuit is calculated as given by,

$$L=\frac{3.33\cdot V_o\cdot(t_{total}-t_{on})}{I_0} \quad (14)$$

In Equation (14), the output current ripple ratio is taken as a constant 0.3 in buck converter design. Therefore, this value can be written as a 3.3 in nominator [23].

The capacitor value which is used in circuit is calculated as given by,

$$C=\frac{V_o\cdot(V_i-V_o)}{8\cdot L\cdot f_s^2\cdot V_i} \quad (15)$$

The output current I_0 of proposed buck converter is calculated from Equation (16).

$$I_0=\frac{V_0}{R} \quad (16)$$

The output voltage can be found by Equation (17).

$$V_o=D\cdot V_i \quad (17)$$

where V_{in} represents input voltage and D is duty cycle of buck converter when all losses are ignored.

An input power of converter can be calculated by Equation (18).

$$P_i=D\cdot V_i\cdot I_0 \quad (18)$$

in which, D represents Duty Cycle, V_{in} stands for input voltage. Channel voltage which is the voltage drop on transistor M_1 when it is conduction is affected I_0. A similar formula is used for calculating output power of converter given as Equation (19).

$$P_o=V_o\cdot I_0 \quad (19)$$

The efficiency of DC-DC Buck Converter is another critical design criterion for proposed structure. After calculating input and output powers of converter, the efficiency can be calculated by Equation (20).

$$\eta=\frac{P_o}{P_i} \quad (20)$$

3. SIMULATION RESULTS

In this section, it is examined input and output powers of systems for each circuit with using PSPICE. The first circuit can be thought of as a classical DC-DC Buck converter without applying a voltage to the bulk terminal.

The second circuit is the structure that has the optimized performance with its proposed circuit part. In this circuit, the V_{BS} voltage is adjusted to 1.2V with the using Voltage divider circuit. This value is determined by simulating V_{BS} voltage for negative and positive V_{BS} voltages. Figure 4 illustrates the V_{BS} voltage which is applied to bulk terminal of M1 and the threshold voltage variation. The value of V_{BS} is specified as 1.2V. This value is the optimized value for the switching performance for M1. A suitable value for V_{BS} is simulated in PSPICE for positive and negative voltages. As a result, the bigger and the smaller bulk terminal voltage values have less efficient on M1 performance for calculated L and C values. Therefore, the best switching performance appears when the V_{BS} value is 1.2 V for this MOSFET parameters. The switching frequency is selected as 20 kHz. To get V_{BS}=1.2V, voltage divider circuit consisting of M2 and M3 has employed as shown in Figure 3. From equation (A), W_3/L_3 is calculated as 29.5 for I_{D3} =65 μA and kn =27.6 μA/V2. Also, W_2/L_2 is calculated as 0.5. The Figure 4 shows the relationship between V_{BS} and threshold voltage of M1. The primary aim of this study is to design a high-efficiency DC-DC buck converter for low power applications. It should be 3.3V source such as portable system, communication systems. All the design parameters are determined according to DC-DC Buckconverter which has the input voltage V_i=10V and output voltage V_o=3.3 V. Then, the inductor value and the capacitor value of Buck Converter are calculated according to formulas (13), (14) successively where C_{iss} is calculated as 131.12 fF. The switching frequency is taken

as 20kHz-100 kHz for switching of M1. The inductor value is calculated and specified as 220 µH and capacitor value is calculated as 40µF. R is selected as 1kΩ. P_{out} is 109 mW, therefore output current will be 33 mA. All these conditions have the effect on working of buck converter and the operation of this circuit structure is directly related with these parameters because, the inductor value should be as small as possible regarding with maximizing output voltage and current. The switching frequency also ought to be selected commonly frequency values. The voltage of M_1 is another critical parameter for operation M_1 safely.

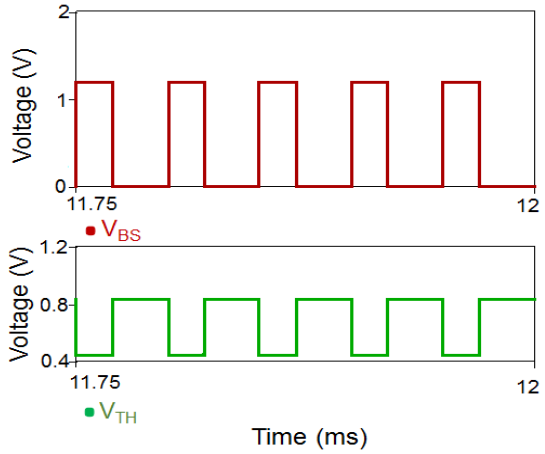

Figure 4. The threshold voltage waveform for proposed buck converter with V_{BS}

This voltage value must be small for getting high performance of MOSFET. All things considered, two circuit structure is simulated via SPICE and the results are evaluated. Figure 5 shows the output voltage of conventional circuit.

It is desired to have the voltage of converter is 3.3 V. This value appears when the duty cycle is 0.395. The theoretical output voltage should be 3.95V when the input voltage 10V.

Figure 6 depicts the output voltage of proposed circuit. The output voltage of this converter is aimed to have 3.3 V. Thisvoltage value occurs when the duty cycle is 0.35. The theoretical output voltage should be 3.5V when the input voltage 10V.

There is a difference between the theoretical and simulation values for conventional buck converter. This is caused by the non-synchronous rectification diode and the current of the converter is small.

Figure 7 displays the output current of proposed circuit. The current of proposed converter is 33 mA when the duty cycle is 0.35.

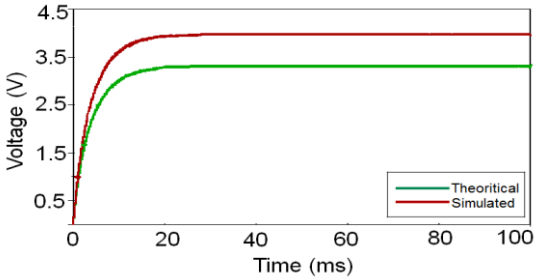

Figure 5. The output voltage of conventional buck converter

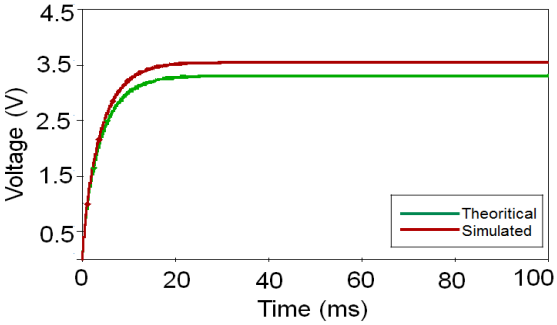

Figure 6. The output voltage of proposed buck converter

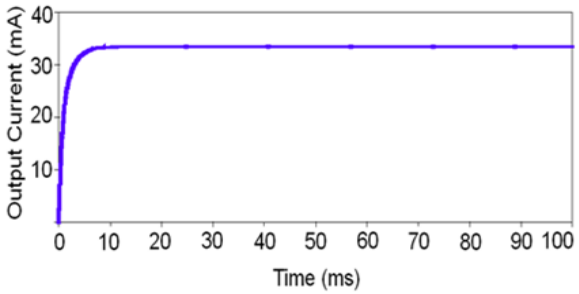

Figure 7. The output current of proposed buck converter

Fig. 8 illustrates the duty cycle- output current characteristics of conventional and proposed circuit designs. It is obvious that when it is compared two circuits, the proposed circuit has higher output current values than conventional circuit.This difference is the effect of applyingbulk-terminal voltage to the bulk terminal of the transistor. With the help of this voltage, the switching performance of the transistor becomes better and the output current of the converter reaches its maximum values compared with conventional circuit. Fig. 9 shows the change in output voltage in two converters for same D value. There is a change in output voltage for proposed circuit. The output voltage should be 10V when the Duty Cycle is taken as 1 since the value of input voltage is 10V, yet this is not same as the Equation (17). The reason for this phenomenon can be explained as the effect of the inductor value, selecting exact value of switching frequency, the voltage of the switching transistor and the diode losses.

The switching frequency also affects the efficiency of the Buck Converter. When the switching frequency increases, there may occur some power consumption owing to high frequency values. The effect on switching frequency is also investigated on the efficiency of the converter. It can be seen that the proposed convertor is more efficient than the conventional converter by applying voltage from bulk terminal. Reducing power consumption with better switching performance is the main goal of this study to increase the total efficiency of the system.

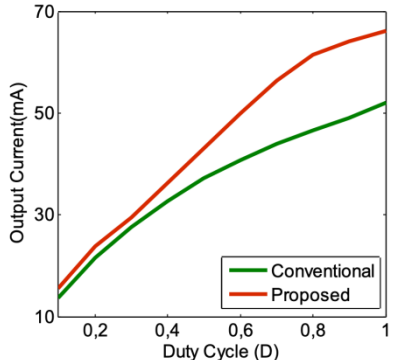

Figure 8. Dutycycle–output current characteristics of two buck converters

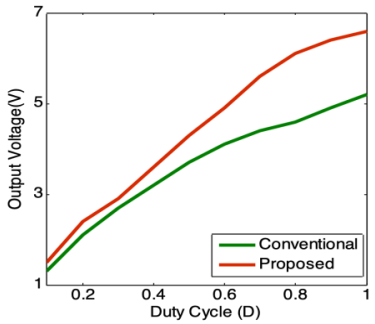

Figure 9. Dutycycle–output voltage characteristics of two buck converters

Figure 10 displays the power consumption distribution on a switching transistor that is simulated in PSPICE. This pattern shows the maximum power dissipation values that the transistor consumes. The Figure 10 A stands for power consumption of switching transistorwhich is used in conventional circuit and the Figure 10 B shows power consumption pattern of switching transistor which is used in proposed circuit. The bulk-terminal voltage on switching transistor has an important impact on power consumption on the converter. The power losses dominantly occur at rising and falling time of switching process for MOSFET. It was calculated the switching power losses in both rising and falling times 7.5 mW and 5mW for classic and proposed buck converters, respectively.

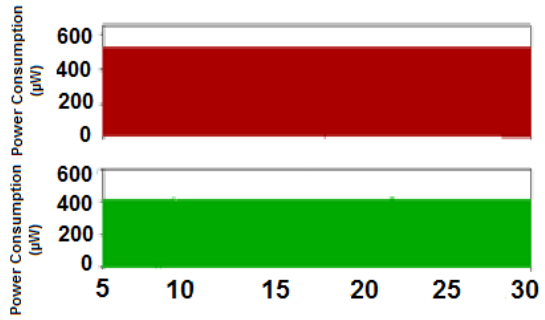

Figure 10. The power consumption distribution on MOSFET

The proposed design increases the efficiency of the suggested structure when it is compared with conventional circuit. This approach would be used in different converter topologies. The main aim of this study is to prove that this design increases the efficiency of the suggested structure when it is compared with conventional circuit.

This approach would be used in different topologies. When it is investigated deeply, the proposed design has larger input voltage/output voltage ratio when it is compared with other converter topologies in Table II. However, minimizing the input voltage can allow having a higher efficiency value for proposed converter. Therefore, the efficiency of novel converter is advantageous in this sense. The converter is also useful as shown in Table II with its simpleness and it is easier to it is easy to control than other converter designs in the literature. The buck proposed converter is advantageous for using in low power applications because it has smaller duty cycle than other converter designs which are listed in Table II. The quantity of power consumption is also another attractive property of this design since it has low power consumption as 1.76 mW. At a first glance, this value seems to be very low when it is taken into consideration the other converter topologies. However, this is reasonable power consumption level for the DC-DC buck converter topology that operates at low power levels. It can also operate at lower duty cycle compared with other converter circuits. The duty cycle of this converter is 0.39. The other converter topologies have bigger duty cycle values than the proposed converter. The exact contribution of this design is to have low power consumption and operate at lower duty cycle compared with other converter topologies in the literature. The output current of buck converter is small in low power applications. Therefore, the output power also becomes small and the efficiency of the converter decreases respectively[30]. The proposed topology is available to develop more stable and efficient converter structure to design more advanced topologies.

3.EXPERIMENTAL RESULTS

The experiments are performed by using two types of MOSFET for both converters. Initially, the classic buck converter with IRLB3034 MOSFET was constructed and some important data are taken to give a detailed form in Table I. The experimental output voltage waveform of the classic buck converter is given in Figure 11.

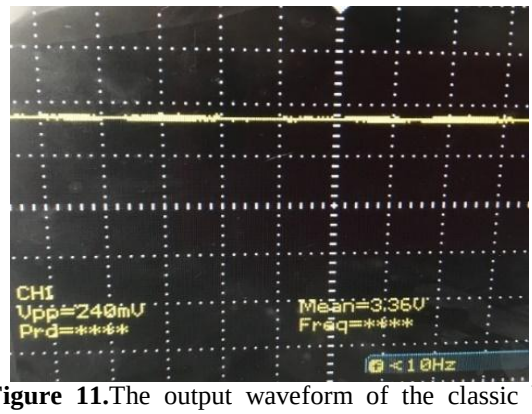

Figure 11. The output waveform of the classic buck converter with the IRLB3034 MOSFET.

In figure 11, the output voltage of this converter is nearly 3.3 V as approved by theoretical approaches. Besides, there appear some undesired ripples on the output voltage of the buck converter. This is an undesirable effect on the performance of the converter. In the second part of the experimental studies, the proposed buck converter was set up by using 4-terminal silicon gate P-Channel

MOSFET (MIC94030). This MOSFET has many advantages in that it has lowresistance value and allows the substrate connection to be distinguished from the source pin. It also has heat management and exhibited low power dissipation during the switching process.The voltage that applied from substrate pin of MIC94030 was calculated from Voltage Divider Circuit. In Fig. 3, there exist two MOSFETs for acting as a resistor.Therefore, it is preferred to use resistors instead of these MOSFETs. To have V_{BS}=1.2V, the resistor values of the Voltage Divider Circuit are specified as R_1=1kΩ and R_2=10KΩ. Theparameters of conventional and proposed buck converters are given in Table 1.

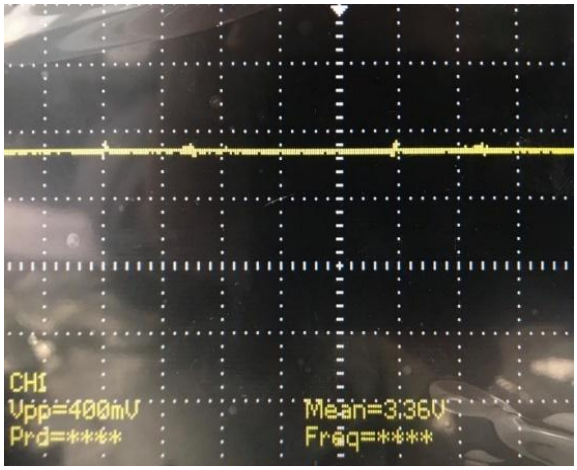

Figure 12. The output waveform of the classic buck converter with the MIC94030 MOSFET.

Figure 12 shows the output waveform of the proposed buck converter with the MIC94030 MOSFET. The output voltage value of the proposed buck converter is approximately obtained 3.3 V which is proved via theoretical results.

The output waveform of the proposed converter has low number of ripples comparing with a conventional buck converter. Also, this converter works at a lower duty cycle when it is set against with conventional buck converter.

Furthermore, the novel converter design is more efficient than the classic buck converter because of the experimental results. This situation provides less power consumption in the converter and this converter performs better than the classic buck converter. Table II illustrates the detailed in formation about these converters. The image of the experimental prototype is given in Figure 13 for proposed the buck converter with 4-pin MIC94030.

Figure 13. The picture of the proposed buck converter with the MIC94030 MOSFET on PCB.

The proposed structure is more efficient than the conventional converter structure for the same values as seen from the Table1.

Table 1. The Specifications for Conventional and Proposed Circuits

	Conventional (Simulation)	**Conventional (Experiment)**	**Proposed (Simulation)**	**Proposed (Experiment)**
MOSFET Type	NMOS	NMOS (IRLB3034)	NMOS	**PMOS (MIC94030)**
Input Voltage	10 V	10 V	10 V	10 V
Inductor	220 µH	220 µH	220 µH	220 µH
Capacitor	40 µF	40 µF	40 µF	40 µF
Output Voltage	3.3 V	3.3 V	3.3 V	3.3 V
Output Current	33 mA	33 mA	33 mA	33 mA
Duty Cycle	0.395	0.41	0.35	0.39
Switching Frequency	20 kHz	20 kHz	20 kHz	20 kHz
Efficiency	82.1	81.5	90.7	88.2
Power Dissipation by MOSFET	1.94 mW	2.44 mW	1.2 mW	1.76 mW

Table 2. Comparison of the Buck Converter Parameters Which Are Selected In Related Papers

	Lindiya [24]	Ito [25]	Woo [26]	Park[27]	Zhang [28]	Su [29]	Proposed
Input Voltage	12V	12 V	1.8 V	2.2V-3.3V	1.8 V	2.5 V	10 V
Inductor (L)	2100 µH	395.8µH	4.7 µH	3 µH	220 µH	N/A	220 µH
Capacitor (C)	100 µF	79.32 µF	4.7 µF	3 µF	1 µF	470 nF	40 µF
Output Voltage	5V	N/A	1V-1.5V	1.7 V	0.3V-0.55 V	0.8V-1.5V	3.3 V
Output Current	N/A	N/A	300 mA	0.01-20 mA	10 mA	8.4 mA	33.6 mA
V_i/V_0 Ratio	2.4	N/A	1.8	1.29	3.27-6	1.66-2.25	3.03
Duty Cycle (D)	0.48	N/A	N/ A	N/A	0.015-0.98	0.5	0.39
Efficiency (%)	N/A	N/A	94	92.4	86	66.7	88.2
Switching Frequency	4.5-4000 kHz	4.4 kHz	1 MHz	2.5 MHz	100 kHz	0.2MHz-1MHz	20 kHz

Table 3. Parameters of MOSFET used in Spice Simulations

MOSFET Model Parameters
MODEL RITSUBN3 NMOS (LEVEL=1 TPG=1 TOX=1.5E-8 LD=2.95E-7 WD=3.00E-7 UO= 726 VTO=1.0 THETA=0.349 RS=27 RD=27 DELTA=2.27 NSUB=1.45E17 XJ=1.84E-7 VMAX=1.10E7 ETA=0.837 KAPPA=0.508 NFS=3E11CGSO=3.4E-10 CGDO=3.48E-10 CGBO=5.75E-10 PB=0.95 XQC=0

The proposed structure is more efficient than the conventional converter structure for the same values as seen from the Table I. The proposed buck converter operates at a lower duty cycle and has low power consumption compared with a conventional buck converter. When it is investigated the Table II, it can be concluded that the duty cycle of the proposed design is lower than [24] and [25]. This corresponds to have higher efficiency for proposed design. This fact shows that the main advantage of the suggested converter is that it allows boosting up the efficiency of the system. The inductor is another parameter for the converter design since it affects the volume of the converter. An input voltage/output voltage ratio is another important parameter which correlates power losses and efficiency. There are also converter topologies which are proposed by Woo [26] and Park [27] has smaller input volt-age/output voltage ratio compared with the proposed circuit. Since this voltage difference between input volt-age and output voltage approximates, it is sensible to reach very high efficiencies in these designs. Since this circuit operates at low power level, the proper efficiency value may not be obtained. Zhang [28] and Su [29] has designed high efficiencies in these designs for digital circuit designs. Since this circuit operates at low power level, the proper efficiency value may not be obtained. Thus, the efficiency level of these designs cannot achieve expected values regarding with other converters in Table-II since the power dissipation of buck converterdecreases with the decline the output current of converter. for proposed design. This fact shows that the ma-in advantage of the suggested converter is that it allows boosting up the efficiency of the system.

The proposed design increases the efficiency of the suggested structure when it is compared with conventional circuit. This approach would be used in different converter topologies. The main aim of this study is to prove that this design increases the efficiency of the suggested structure when it is compared with conventional circuit.

This approach would be used in different topologies. When it is investigated deeply, the proposed design has larger input voltage/output voltage ratio when it is compared with other converter topologies in Table II. However, minimizing the input voltage can allow having a higher efficiency value for proposed converter. There-fore, the efficiency of novel converter is advantageous in this sense. The converter is also useful as shown in Table II with its simpleness and it is easier to it is easy to control than other converter designs in the literature. The buck proposed converter is advantageous for using in low power applications because it has smaller duty cycle than other converter designs which are listed in Table II. The quantity of power consumption is also another attractive property of this design since it has low power consumption as 1.76 mW. At a first glance, this value seems to bevery low when it is taken into consideration the other converter topologies. However, this is reasonable power consumption level for the DC-DC buck converter topology that operates at low power levels. It can also operate at lower duty cycle compared with other converter circuits.

The duty cycle of this converter is 0.39. The other con-verter topologies have bigger duty cycle values than the proposed converter. The exact contribution of this de-sign is to have low power consumption and operate at lower duty cycle compared with other converter topologies in the literature. The output current of buck converter is small in low power applications. Therefore, the output power also becomes small and the efficiency of the converter decreases respectively [30]. The proposed topology is available to develop more stable and efficient converter structure to design more advanced topologies.

4. CONCLUSIONS

In this work, a highly efficient and simple DC-DC Buck Converter is simulated and designed for mobile applications and microcontroller circuits with output voltage 3.3 V and input voltage 10V. The simulations and experiments are performed to validate the efficiency and performance of both converters. The simulations are performed in PSPICE for conventional and proposed circuits. Also, the experiments are performed for classic and proposed boost converter successively. The pro-posed converter efficiency is reasonable considering its simple circuit structure. It is concluded that the efficiency of the DC-DC Buck Converter increases with a applying bulk-terminal voltage signal on a MOSFET. The pro-posed buck converter operates at a lower duty cycle and has low power consumption. This is the result of the threshold voltage effect on MOSFET performance. The size of buck converter circuit elements is also minimized by specifying the proper switching frequency, the value of inductor and the value of capacitor. The efficiency of the converter will be improved by using different circuit structures which are low-power consumption. This topology is also suitable for CMOS integrated circuit structure. In conclusion, this proposed design can be used in microprocessors, portable devices, solar systems and embedded integrated circuits.

REFERENCES

[1] M. H. Rashid, *Power Electronics Handbook*, Aca. Pre. Ser. in Eng. 2011.

[2] N. Safari, Design of a DC/DC buck converter for ultra-low power applications in 65nm CMOS Process, Master thesis in Department of Electrical Engineering, Linköping Institute of Technology, 2012:54.

[3] İ.Büyükkeskin, , S. A.Tekin, , S.Gürel, M. S. Genç, Electricity Production from Wind Energy By Piezoelectric Material. *International Journal of Renewable Energy Development*, 8(1), pp41-46, 2019.

[4] S. Evanczuk, "Buck Converters Simplify Energy Harvesting from High-Input-Voltage-Transducers". *Digi-key Electronics*,vol 1, 2013.

[5] M. Z. Hossain, N. A. Rahim, J. L. Selvaraj, Recent progress and development on power DC-DC converter topology, control, design, and applications: A review, *Renewable and Sustainable Energy Review*, vol.81, pp.205-230, 2017.

[6] C. Hua, Y. A. Deng, A Novel Dual-Bridge LLC Resonant Converter with Wide Range of Low Input Voltage", *Energy Procedia*, pp.361-365,2019.

[7] N. Zhang, D. Sutanto and K. M. Muttaqi, "A review of topologies of three-port DC–DC converters for the integration of renewable energy and energy storage system", *Renewable and Sustainable Energy Review*, vol.56, pp.388-40, 2015.

[8] D. Guilbert, S. M. Collura, A. Scipioni, DC/DC converter topologies for electrolyzers: State-of-the-art and remaining key issues, *International Journal of Hydrogen Energy*, vol.42,pp.23966-23985, 2017.

[9] S. Arruugam, P. Logmani, Modeling and adaptive control of modified LUO converter, *Microprocessors and Microsystems*, vol. 56, 102889, 2019.

[10] A. Amir, A. Amir, H. S. Che, A. Elkhateb, N. A. Rahim,Comparative analysis of high voltage gain DC-DC converter topologies for photovoltaic systems, *Renewable Energy*, vol.136, pp.1147-1163,2018.

[11] J. S. Lopez, I. P. F. Donoso, L. M. F. Morais, P. C. Cortizo, M. A. Sever, Digital control strategy for a buck converter operating as a battery charger for stand-alone photovoltaic systems, *Solar Energy*, vol.140, pp.473-487, 2016.

[12] H. Luo, H. Wen, X. Li, L. Jiang, Y. Hu, Synchronous buck converter based low-cost and high-efficiency sub-module DMPPT PV system under partial shading conditions, *Energy Conversion and Management*, vol.126, pp.473-487,2016.

[13] M. Gupta, S. p. Phulambrikar," Design and analysis of Buck Converter", *International Journal of Engineering Research and Technology*, vol.3, no.3, pp.2346-2350, 2014.

[14] F. Khateb, Bulk-driven floating-gate and bulk-driven quasi-floating gate techniques for low-voltage low-power analog circuit design., *AEU- International Journal of Electronics and Communications*, vol.68, no.1, pp.64-72, 2014.

[15] J. F. Da Rocha, N. B. Dos Santos, J. M. D. Costa, Voltage Spikes in Integrated CMOS Buck DC-DC Converters: Analysis for Resonant and Hard Switching Topologies, *Procedia Technology*, vol.17, pp.327-334,2014.

[16] V. R. K. Kanamarlapudi, B. Wang, N. K. Kandasamy, P. L. So, A New ZVS Full-Bridge DC–DC Converter for Battery Charging with Reduced Losses Over Full-Load Range, *IEEE Transactions on Industry Applications*, vol.54, no.6, pp. 571-579,2018.

[17] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, High Conversion Ratio DC–DC Converters with Reduced Switch Stress, *IEEE Transactions on Circuits and Systems-I, Regular Paper*, vol.55, no.7,pp.2139-2151,2008.

[18] D. Oulad-Abbou, S. Doubabi, A. Rachid, Power switch failures tolerance of a photovoltaic fed three-level boost DC-DC converter, *Microelectronics Reliability*, vol.92, pp.87-95, 2018.

[19] Khateb, D. Biolek, "Bulk-Driven Current Differencing Transconductance Amplifier,*Circuits, Systems, and Signal Processing*, vol.30, pp.1071-1089, 2011.

[20] S. Gurel, S. A. Tekin, "The New Approach for Switching Performance of Power MOSFET", *Innovative Applications in Engineering*, pp. 95-100, 2018.

[21] H. Ercan, S. A. Tekin, M. Alçı, "Low-voltage low-power multifunction current-controlled conveyor", *International Journal of Electronics*, vol.102, no. 3, pp. 444-461, 2014.

[22] A. S. Sedra, K. C. Smith, T. C. Carusone, V. Gaudet, *Microelectronic Circuits*, New York: Oxford University Press, 2016.

[23] Power MOSFET Basics: Understanding Gate Charge andUsing it to Assess Switching Performance.*VISHAY SILICONIX, Device Application Note AN698A*. pp.1-6,2016.

[24] A. Lindiya, D. S. Palani, a. Iyyappan, Performance Comparison of Various Controllers for DC-DC Synchronous Buck Converter, *Procedia Engineering*, vol.38, pp.2679-2693, 2012.

[25] D. Ito, H. Asahara, T. Kousaka, T. Ueta, Clock pulse modulation for ripple reduction in-buck-converter circuits, *Chaos, Solitons & Fractals*, vol.111, pp.138-145, 2018.

[26] X. Zhang, P. Chen, Y. Okama, K. Ishida, Y. Ryu, K. Watanabe, T. Sakurai, M. Takamiya, A 0.6 V Input CCM/DCM Operating Digital Buck Converter in 40 nm CMOS, *IEEE Journal of Solid -State Circuits*, vol.49, no.11, pp.2377-2386,2014.

[27] L. Su, D. Ma, A. P. Brokaw, Design and Analysis of Monolithic Step-Down SC Power Converter With Subthreshold DPWM Control for Self-Powered Wireless Sensors, *IEEE Transactions on Circuits and Systems-I :Regular Papers*, vol.57, no.1, pp. 280-290, 2010.

[28] K. Woo, Y. Oh, B. Yang, "DC-DC Buck Converter Using Analog Coarse-Fine Self-Tracking Zero-Current Detection Scheme", *IEEE Transactions on Circuits and Systems-II:Express Briefs*, vol.66, no.11, pp.1850-184, 2019.

[29] Y Park, H. Kim, S. Kim, Y. Pu, K. Hwang, Y. Yang, M. Lee, K. Lee, A Design of a 92.4% Efficiency Triple Mode Control DC–DC Buck Converter with Low Power Retention Mode and Adaptive Zero Current Detector for IoT/Wearable Applications, *IEEE Transactions on Power Electronics*, vol.32, no. 9, pp.6946-6960, 2017.

[30] F. Santoro, R. Kuhn, N. Gibson, N. Rasera, T. Tost, D. Schmitt-Landsiedel, R. Brederlow, "A 92.1% Efficient DC-DC Converter for Ultra-Low Power Microcontrollers with Fast Wake-up" *2017 IEEE Custom Integrated Circuits Conference*, pp. 1-4, 2017.